

CLAIMS

What is claimed is:

- 5 1. An integrated circuit, comprising:
 an array of function blocks, wherein each function block has an input and
 an output;
 a predesigned routing structure formed over the array, including:
 a plurality of vertical tracks,
10 wherein, in a first conducting layer of the predesigned
 routing structure, each track includes a pin in communication with
 a respective input or output and
 wherein, in the first conducting layer, each track further
 includes a first vertical conductor, uncoupled to the pin.
- 15 2. The integrated circuit of claim 1, wherein a second vertical conductor is
 formed in a second conducting layer, wherein the second vertical conductor is
 coupled to the first vertical conductor, but is uncoupled to the pin.
- 20 3. The integrated circuit of claim 2, wherein the second vertical conductor is
 formed substantially under the pin.
4. The integrated circuit of claim 1, further including a plurality of horizontal
 conductors that are formed under the first vertical conductors.
- 25 5. The integrated circuit of claim 1, further including a customized conducting
 layer, wherein some conductors in the customized conducting layer are coupled to
 respective pins in the first conducting layer and other conductors in the customized
 conducting layer are coupled to respective first vertical conductors.

6. The integrated circuit of claim 1, further including:

a customized conducting layer formed over the predesigned routing structure, wherein a first portion of the customized conducting layer formed over the pins is for local routing and a second portion of the customized conducting layer is for global routing.

7. The integrated circuit of claim 1, further including:

a customized conducting layer formed over the predesigned routing structure and including a power line and a ground line.

8. The integrated circuit of claim 1, wherein the predesigned routing structure is independent of any channels and is formed over each of the function blocks, wherein each function block remains usable.

9. The integrated circuit of claim 1, further including:

a plurality of conductors for carrying at least one clock signal, wherein the plurality of conductors are uncoupled to the pins or vertical conductors, and

wherein the plurality of conductors can be coupled with a custom conducting layer to form multiple independent clock domains.

10. An integrated circuit, comprising:

an array of function blocks, wherein each function block has an input and an output;

a predesigned routing structure formed over the array, wherein the predesigned routing structure includes a plurality of conducting layers that include a plurality of pins and a plurality of unbroken conductive paths,

wherein each pin is in communication with a respective input or output,

wherein the structure includes a plurality of tracks, and

wherein in each track is located at least a portion of at least one respective unbroken conductive path and at least one respective pin in one of the plurality of conducting layers, and wherein the unbroken conductive path is uncoupled to the respective pin.

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11. The integrated circuit of claim 10, wherein each unbroken conductive path is formed on two conducting layers.

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12. The integrated circuit of claim 10, wherein each unbroken conductive path is formed on two conducting layers and wherein a portion of each unbroken conductive path is formed substantially under the pin located in the same track as the unbroken conductive path.

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13. The integrated circuit of claim 10, further including a customized conducting layer, wherein the customized conducting layer couples first selected pins to selected unbroken conductive paths, second selected pins to other selected pins, third selected pins to a power line, and fourth selected pins to a ground line.

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14. The integrated circuit of claim 10, further including:
a customized conducting layer formed over the predesigned routing structure and including a power line and a ground line, wherein the power line and the ground line are placed so as not to prevent the coupling of an unbroken conductive path to a pin by the customized conducting layer.

15. The integrated circuit of claim 10, further including:

a customized conducting layer formed over the predesigned routing structure, wherein a first portion of the customized conducting layer formed over the pins is for local routing and a second portion of the customized conducting layer is for global routing.

16. The integrated circuit of claim 10, further including:

a plurality of conductors for carrying at least one clock signal, wherein the plurality of conductors are uncoupled to the pins or unbroken conductive paths, and wherein the plurality of conductors can be coupled with a custom conducting layer to form multiple independent clock domains.

17. An integrated circuit, comprising:

an array of function blocks, wherein each function block has an input and an output;

a predesigned routing structure formed over the array, including:

a first conducting layer having a plurality of parallel vertical tracks, wherein included in each track is a pin in communication with a respective input or output and in each track is a first portion of an unbroken conductive path, wherein the pin and the first portion are uncoupled to one another;

for each track, a second portion of the unbroken conductive path, wherein the second portion is formed in at least one other conducting layer.

18. The integrated circuit of claim 17, wherein the second portion is formed substantially under the pin for the respective track.

19. The integrated circuit of claim 17, wherein the unbroken conductive path runs the vertical height of a function block.

20. The integrated circuit of claim 17, wherein the unbroken conductive path is longer than the pin.

21. The integrated circuit of claim 17, wherein for every other track in the first
5 conducting layer, the second portion of the unbroken conductive path is formed in a second conducting layer under the first conducting layer, for the remaining tracks, the second portion of the unbroken conductive path is formed in a third conducting layer under the second conducting layer.

10 22. The integrated circuit of claim 17, wherein:
the predesigned routing structure further includes horizontal conductors formed under the first portion of the unbroken conductive paths and in communication with the first conducting layer.

15 23. The integrated circuit of claim 17, further including a customized conducting layer wherein the customized conducting layer includes conductors that are coupled to the first conducting layer and wherein the customized conducting layer is used to form a user-defined circuit on the integrated circuit.

20 24. The integrated circuit of claim 17, further including a customized conducting layer formed over the predesigned routing structure, wherein a first portion of the customized conducting layer formed over the pins is for local routing and a second portion of the customized conducting layer is for global routing.

25 25. The integrated circuit of claim 17, further including:
a customized conducting layer formed over the predesigned routing structure and including a power line and a ground line, wherein the power line and the ground line are placed so as not to prevent the coupling of an unbroken conductive path to a pin by the customized conducting layer.

26. The integrated circuit of claim 17, including:

a plurality of conductors for carrying at least one clock signal, wherein the plurality of conductors are uncoupled to the pins or vertical conductors, and wherein the plurality of conductors can be coupled with a custom conducting layer to form multiple independent clock domains.

27. An integrated circuit, comprising:

an array of function blocks, to be used in the formation of a user-defined circuit, wherein each function block includes a device layer and at least one device interconnect layer, and wherein each function block has an input and an output;

a routing structure formed over the array including four conducting layers, wherein:

a first predesigned conducting layer including a plurality of parallel vertical tracks, wherein each track includes a pin in communication with a respective input or output, and wherein each track includes a first portion of an unbroken conductive path, wherein the pin and the first portion of the unbroken conductive path are uncoupled to one another;

a second predesigned conducting layer formed under the first conducting layer, wherein for a first group of alternate vertical tracks in the first conducting layer, the second conducting layer includes a second portion of each unbroken conductive path, wherein the second portion is in communication with the respective first portion and is formed substantially under the respective pin,

a third predesigned conducting layer formed under the second conducting layer, wherein for a second group of alternate vertical tracks in the first conducting layer, the third conducting layer includes a second portion of each unbroken conductive path, wherein the second portion is in communication with the respective first portion and is formed substantially under the respective pin, and

a customized conducting layer formed over the first predesigned conducting layer and in communication with the first conducting layer, wherein the customized conducting layer has been formed in accordance with a user-defined circuit.

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28. The integrated circuit of claim 27, wherein:
the second predesigned conducting layer includes horizontal conductors in communication with the first conducting layer.

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29. The integrated circuit of claim 27, wherein the customized conducting layer includes a power line and a ground line, wherein the power line and the ground line are placed so as not to prevent any desired coupling of an unbroken conductive path to a pin by the customized conducting layer.

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30. The integrated circuit of claim 27, wherein:
the customized conducting layer has been formed into a local routing portion and a global routing portion.

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31. The integrated circuit of claim 30, wherein:
the local routing portion is formed over the area occupied by the pins of the first conducting layer.

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32. The integrated circuit of claim 27, wherein:
the second predesigned conducting layer includes conductors for use in clock distribution.

33. The integrated circuit of claim 27, wherein:
the second predesigned conducting layer includes conductors for use in clock distribution wherein the conductors for use in clock distribution can be

coupled by a customized conducting layer to form multiple independent clock domains.

34. An integrated circuit, comprising:

5 an array of function blocks, wherein each function block has an input and an output;

a predesigned routing structure formed over the array, wherein the routing structure includes a plurality of clock conductors, wherein the clock conductors can be coupled with a custom layer to form multiple independent clock domains.

35. The integrated circuit of claim 34, wherein over each function block are formed four clock conductors, where a first clock conductor extends vertically upwards, a second clock conductor extends vertically downwards, a third clock conductor extends horizontally to the right, and a fourth clock conductor extends horizontally to the left.

36. The integrated circuit of claim 34, further including the custom layer, wherein the four clock conductors in a first function block are coupled to form a first clock tree, and wherein the four clock conductors in a second function clock are coupled to form a second clock tree.

37. An integrated circuit, comprising:

25 an array of function blocks, wherein each function block has an input and an output;

a predesigned routing structure formed over the array, including:

a first conducting layer having a plurality of parallel vertical tracks, wherein included in each track is a pin in communication with a respective input or output and in each track is a first portion of an unbroken

conductive path, wherein the pin and the first portion are uncoupled to one another;

for each track, a second portion of the unbroken conductive path, wherein the second portion is formed in at least one other conducting layer;

5 a plurality of clock conductors, wherein the clock conductors can be coupled with a customized conducting layer to form multiple independent clock domains.

10 38. The integrated circuit of claim 37, wherein the second portion is formed substantially under the pin for the respective track.

39. The integrated circuit of claim 37, wherein the unbroken conductive path runs the vertical height of a function block.

15 40. The integrated circuit of claim 37, wherein the unbroken conductive path is longer than the pin.

20 41. The integrated circuit of claim 37, wherein for every other track in the first conducting layer, the second portion of the unbroken conductive path is formed in a second conducting layer under the first conducting layer, for the remaining tracks, the second portion of the unbroken conductive path is formed in a third conducting layer under the second conducting layer; and

wherein the plurality of clock conductors are formed in the second conducting layer.

25 42. The integrated circuit of claim 37, further including the customized conducting layer, wherein the customized conducting layer includes conductors that are coupled to the first conducting layer and wherein the customized conducting layer is used to form a user-defined circuit on the integrated circuit.

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43. The integrated circuit of claim 37, wherein the plurality of clock conductors includes four clock conductors in a second conducting layer formed under the first conducting layer, wherein the four conductors are uncoupled to one another in the second conducting layer.

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